What is claimed is:

1. A method of manufacturing a non-volatile memory device comprising:

forming a tunnel oxide layer on a semiconductor substrate having a self-aligned shallow trench isolation;

depositing a first floating gate layer on the tunnel oxide layer at a first temperature of no less than about 530°C; and

in-situ depositing a second floating gate layer on the first floating gate layer at a second temperature of no more than about 580°C.

2. The method as claimed in claim 1, wherein the first floating gate layer comprises either doped polycrystalline silicon or undoped polycrystalline silicon.

3. The method as claimed in claim 1, wherein the second floating gate layer comprises either doped amorphous silicon or undoped amorphous silicon.

4. The method as claimed in claim 1, wherein the first temperature is in the range of approximately 530°C to 650°C.

5. The method as claimed in claim 1, wherein the second temperature is no more than about 550°C.

6. A method of manufacturing a non-volatile memory device comprising:

forming a tunnel oxide layer on a semiconductor substrate having a self-aligned shallow trench isolation;

loading the substrate into a piece of deposition equipment;

depositing a doped polycrystalline silicon on the tunnel oxide layer while introducing a first doping gas in the deposition equipment at a first temperature of more than about 530°C to thereby form a first floating gate layer;

in-situ depositing a doped amorphous silicon on the first floating gate layer while introducing a second doping gas in the deposition equipment at a second temperature of less than about 580°C to thereby form a second floating gate layer; and

unloading the substrate from the deposition equipment.

7. The method as claimed in claim 6, wherein the first and second doping gases comprise a phosphine (PH_3) gas.

8. The method as claimed in claim 6, wherein the first and second floating gate layers are deposited in a single processing chamber.

9. The method as claimed in claim 6, wherein the first floating gate layer is deposited in a first processing chamber of the deposition equipment and the second floating gate layer is deposited in a second processing chamber of the deposition equipment.

10. A method of manufacturing a non-volatile memory device comprising:

forming a tunnel oxide layer on a semiconductor substrate having a self-aligned shallow trench isolation;

loading the substrate into a piece of deposition equipment;

depositing an undoped polycrystalline silicon on the tunnel oxide layer at a first temperature of no less than about 530°C to thereby form a first floating gate layer;

in-situ depositing a doped amorphous silicon on the first floating gate layer while introducing a doping gas in the deposition equipment at a second temperature of no more than about 580°C to thereby form a second floating gate layer; and

unloading the substrate from the deposition equipment.

11. The method as claimed in claim 10, wherein the doping gas comprises a phosphine (PH_3) gas.

12. The method as claimed in claim 10, wherein the first and second floating gate layers are deposited in a single processing chamber.

13. The method as claimed in claim 10, wherein the first floating gate layer is deposited in a first processing chamber of the deposition equipment and the second floating gate layer is deposited in a second processing chamber of the deposition equipment.

14. A method of manufacturing a non-volatile memory device comprising:

forming a tunnel oxide layer on a semiconductor substrate having a self-aligned shallow trench isolation structure;

loading the substrate into a piece of deposition equipment;

depositing an undoped polycrystalline silicon on the tunnel oxide layer at a first temperature of no less than about 530°C to thereby form a first floating gate layer;

in-situ depositing an undoped amorphous silicon on the first floating gate layer at a second temperature of no more than about 580°C to thereby form a second floating gate layer;

unloading the substrate from the deposition equipment; and

ion-implanting a dopant on the substrate on which the second floating gate layer is formed, to thereby dope the first and second floating gate layers with the dopant.

15. The method as claimed in claim 14, wherein the dopant comprises either phosphorus (P) or boron (B).

16. The method as claimed in claim 14, wherein the first and second floating gate layers are deposited in a single processing chamber.

17. The method as claimed in claim 14, wherein the first floating gate layer is deposited in a first processing chamber of the deposition equipment and the second floating gate layer is deposited in a second processing chamber of the deposition equipment.

18. The method as claimed in claim 14, further comprising the step of performing a heat treatment to activate the dopant, after doping the first and second floating gate layers.

19. The method as claimed in claim 18, wherein the heat treatment is carried out at a temperature of no less than about 300°C.

20. A non-volatile memory device having a self-aligned shallow trench isolation structure including a floating gate having sidewalls and a surface, said sidewalls being perpendicular to said surface.

21. A method of manufacturing a non-volatile memory device comprising:

forming a self-aligned shallow trench isolation device having a temporary floating gate with walls that have a positive slope;

removing said temporary first floating that has walls with a positive slope; and

forming a permanent floating gate layer that has walls perpendicular to its surface.

22. The method recited in claim 21, wherein said permanent floating gate layer is made of doped polycrystalline.

23. The method recited in claim 22, wherein said permanent floating gate layer is deposited at a high temperature of more than about 580°C.

24. The method recited in claim 23, further including the step of depositing a second floating gate layer.

25. The method recited in claim 24, wherein said second floating gate layer made of a doped polycrystalline and is deposited at a temperature of about 530°C.

26. The method recited in claim 21, wherein said temporary floating gate is removed by a dry etching process.

27. The device recited in claim 20, wherein said floating gate comprises doped polycrystalline silicon or undoped polycrystalline silicon.

28. The device recited in claim 20, including a second floating gate layer.

29. The device recited in claim 28, wherein said second floating gate layer comprises either doped amorphous silicon or undoped amorphous silicon.

30. The device recited in claim 20, including a tunnel oxide layer.

31. The method recited in claim 24, wherein said second floating gate layer is in-situ deposited to prevent the growth of a native oxide layer on the surface of said permanent floating gate layer.